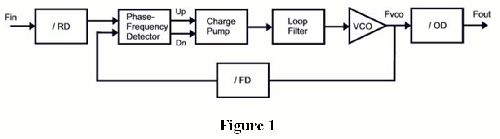
**What is PLL?**

A phase-locked loop (PLL) is an electronic circuit with a voltage or voltage-driven oscillator that constantly adjusts to match the frequency of an input signal. It is easy to initially visualize as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal, and the phase detector compares the phase of that signal with the phase of the input periodic signal, adjusting the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is "fed back" toward the input forming a loop.

**Architecture of PLL:**



**Description of the architecture:**

A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a VCO which creates an output phase. The output is fed through an optional divider back to the input of the system, producing a negative feedback loop. If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase at the other input. This input is called the reference.

Analog phase locked loops are generally built with an analog phase detector, low pass filter and VCO placed in a negative feedback configuration. A digital phase locked loop uses a digital phase detector; it may also have a divider in the feedback path or in the reference path, or both, in order to make the PLL's output signal frequency a rational multiple of the reference frequency. A non-integer multiple of the reference frequency can also be created by replacing the simple divide-by-N counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.

The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. If the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator so that it speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs.

Depending on the application, either the output of the controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system.

**How it works:**

PLLs work by constantly adjusting a voltage or current-driven oscillator to match (lock onto) the phase and frequency of an input signal, which typically consists of a voltage-controlled oscillator (VCO) tuned using a special semiconductor diode called a varactor. The VCO is initially tuned to a frequency close to the desired receiving or transmitting frequency. A circuit called a phase comparator causes the VCO to seek and lock onto the desired frequency, which is set via a crystal-controlled reference oscillator. When the VCO frequency differs from the reference frequency, the phase comparator produces an error voltage. The comparator output is usually run through a low-pass filter (a signal filter that reduces the strength of high-frequency waves) to further reduce noise. The filtered output is fed back to the varactor to continually push the VCO toward the reference frequency. The filtered output of the comparator also provides the output of the circuit -- the signal found in the transmission (the voice, video or data). Since the signal is encoded by modulating a carrier wave, it can be thought of as the difference between the carrier waveform and the actual transmitted waveform, and can therefore be found in the output of the comparator.

**Advantage of PLL:**

1. PLL systems are very important in generating accurate and stable frequency
2. Locking characteristic is a very important feature in PLL system. A PLL oscillator locked to a reference harmonic offers a very low phase noise defined by that reference.

**Limitations of PLL:**

* PLLs use a negative-feedback control system similar to that of an amplifier, so the concepts of loop bandwidth and phase margin apply here as well.

**Solve:** Generally, the loop bandwidth should be set smaller than one-tenth of the PFD frequency, and the safe range for phase margin is from 45° to 60°

* There is a problem in PLL that the slew rate is high

**Solve:** to solve it we keep the capacitance in parallel with the input port small, as it will decrease the slew rate of the incoming signal

* If the impedance at the reference input doesn’t match with the PLL then error may arise.

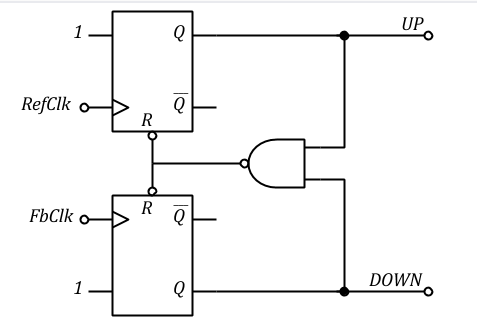
**Solve**: We need to match the impedance at the reference input port of the PLL in order to minimize reflections.

**What is PFD?**

PLL often includes a phase frequency detector (PFD) to monitor the phase and frequency differences between its two inputs and transfers the information to the charge pump generating the voltage signal that controls the frequency of the voltage-controlled oscillator.

A phase frequency detector (PFD), in electronics, is a device which compares the phase of two input signals. It has two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and another from some external source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase.

**ARCHITECTURE OF PFD:**

**DESCRIPTION:**

Outputs digital pulses whose widths are proportional to the phase difference between RefClk and FbClk

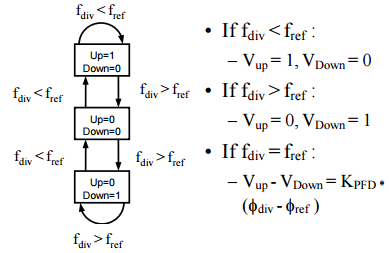
Time domain waveforms, ref leading, ref lagging, with clock slips

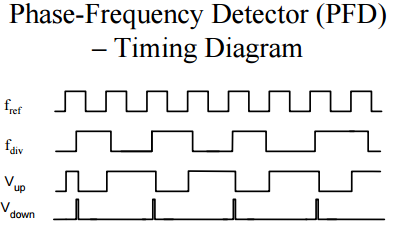
Edge triggered, sensitive only to rising or falling edges of RefClk and FbClk

Ideally should be independent of duty-cycle of clocks

State diagram of PFD which is sensitive to rising edge of RefClk clock

**HOW IT WORKS?**





**CHARACTERISTICS OF PFD:**

• Tri-state PFD

• Edge-Triggering Circuits Are Used to Eliminate dependency of Gain to Input Duty Cycle

• Nominal Output Frequency is same as Reference

• Two Outputs are Subtracted => Output Has Three Possible States: –1, 0, 1

• Locked-State Phase Error is 0 Degree => Small pulses at Outputs => Low Power, Low Noise

**LIMITATIONS OF PFD**:

1. **DEAD ZONE:**

Digital PFD exhibit a region of small or zero gain near the phase lock. This low gain region is commonly known as the dead zone. The main cause of dead zone is the relationship between the propagation delay of the internal gates for the reset of the PFD and the switching time of the charge pump currents.

When VCO frequency differs slightly from reference oscillator phase, the PFD should be able to generate short pulse to steer the VCO back to it’s intended frequency. If not, then VCO frequency can fluctuate randomly in that region.

Usage of Tri state PFD with delay logic added to reset path.

We can solve this by making the delay in the rest path to be longer than the switching time of the charge pump currents.

2) **BLIND ZONE:**

The frequency insensitivity of the PFD to any transitions in the input signals in known as blind zone. This blind zone induces wrong polarity in the PFD output, leading to incorrect behavior and increasing the acquisition time. At high frequency, particularly in the PLLs used for optical communication, this is a major problem.

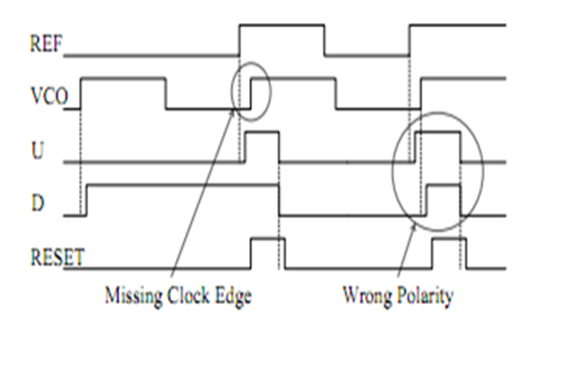
This blind zone degrades the maximum phase detection range (ømax) of the PFD.

ømax =2π(1 – Tr x fin)……….[1]

One way is to reduce Tr. But it is not possible to remove reset time. Hence, it is not possible to eliminate blind zone. This will lead to poor frequency sensitivity and low phase detection range.

1. **MISSING EDGE:**

A rising edge of the VCO clock arrives far earlier than that of the reference clock, thus the PFD activating the D signal shown in the figure. As the reset pulse overrides the rising edge, the PDF does not detect this rising edge.



Hence it does not activate D signal that should be generated for the missing edge. In addition, the PFD activates the up signal when the rising edge of the reference clock arrives later.

Therefore, a missing edge makes the PFD output being reversed in polarity, enlarging the acquisition time of the PLL.

**APPLICATION OF PFD:**

Analog Devices phase frequency detectors offer high performance and ultralow phase noise in a low cost, compact package. This device can significantly improve frequency lock time, and include automatic and configurable lock detect indicators.

PFD can be used for:

• Point-to-point radios

• Satellite communications

• Military

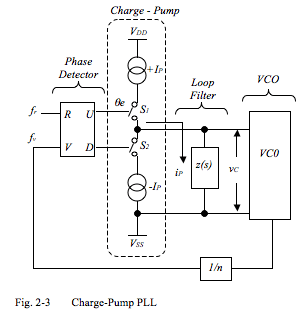
• SONET clock generation

**What is charge pump?**

A charge pump is a kind of DC to DC converter that uses capacitors as energy-storage elements to create either a higher- or lower-voltage power source. A charge pump IC converts, and optionally regulates, voltages using switching technology and capacitive-energy storage elements. Charge pumps offer high-efficiency and compact solutions for applications with generally low-output current requirements.

The output frequency is given by. The charge-pump PLL (CP-PLL) is an extension of the basic PLL requiring the addition of a charge-pump between the phase detector and loop-filter. A specific embodiment uses a three-state phase detector (3PD) which is used for the analysis going forward.

**Architecture of Charge pump:**



**Description:**

We describe the fundamental properties of a charge-pump PLL (CP-PLL). The CP-PLL derives its name from the fact that the phase detector (PD) output is a current source as opposed to a voltage source and "pumps" current into and out of the loop-filter. This form of PLL is popular because it is adaptable to integration in microcircuit devices.

**How it works:**

**Limitations of Charge Pumps:**

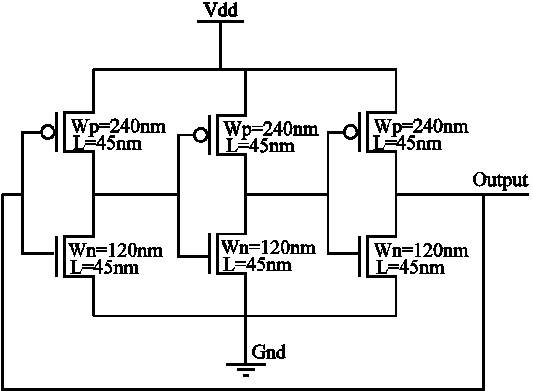
* Leakage current: Small currents that flow when the switch is off.
* Mismatches in the Charge Pump: The up and down (charge and discharge) currents are unequal.
* Timing Mismatch in PFD: Any mismatch in the time at which the PFD provides the up and down outputs.
* Charge Sharing: The presence of parasitic capacitors will cause the charge on the desired capacitor to be shared with the parasitic capacitors.

**What is Voltage Controlled Oscillator?**

A voltage controlled oscillator (VCO) is one of the most important basic building blocks in analog and digital circuits [1]-[6]. There are many different implementations of VCOs. One of them is a ring oscillator based VCO, which is commonly used in the clock generation subsystem. The main reason of ring oscillator popularity is a direct consequence of its easy integration.

A Voltage controlled oscillator is an oscillator with an output signal whose output can be varied over a range, which is controlled by the input DC voltage. It is an oscillator whose output frequency is directly related to the voltage at its input. The oscillation frequency varies from few hertz to hundreds of GHz. By varying the input DC voltage, the output frequency of the signal produced is adjusted.

**Architecture of VCO**:



**Description of the schematic:**

Here we use a three stage VCO using CS amplifier ring oscillator. There are 3 Nmos and 3 pmos. The poms are connected together with a triode load. The output of first cmos is the input of 2nd cmos and the output of 2nd coms is the input of 3rd coms. The output of the last Cmos is connected to the input of the 1st cmos which is the input. There are three parasitic capacitor connected at the output of the cmos.

**How VCO works?**

A ring oscillator is comprised of a number of delay stages, with the output of the last stage feed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining phase shift is provided by a dc inversion. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped.

In a device fabricated with MOSFETs, for example, the gate capacitance must be charged before current can flow between the source and the drain. Thus, the output of every inverter in a ring oscillator changes a finite amount of time after the input has changed. From here, it can be easily seen that adding more inverters to the chain increases the total gate delay, reducing the frequency of oscillation. The ring oscillator is a member of the class of time delay oscillators. A time-delay oscillator consists of an inverting amplifier with a delay element between the amplifier output and its input. The amplifier must have a gain greater than 1 at the intended oscillation frequency. Consider the initial case where the amplifier input and output voltages are momentarily balanced at a stable point. A small amount of noise can cause the amplifier output to rise slightly. After passing through the time-delay element, this small output voltage change will be presented to the amplifier input. The amplifier has a negative gain of greater than 1, so the output will change in the direction opposite to this input voltage. It will change by an amount larger than the input value, for a gain greater than 1. This amplified and reversed signal propagates from the output through the time-delay and back to the input where it is amplified and inverted again. The result of this sequential loop is a square-wave signal at the amplifier output with the period of each half of the square wave equal to the time delay. The square wave will grow until the amplifier output voltage reaches its limits, where it will stabilize. A more exact analysis will show that the wave that grows from the initial noise may not be square as it grows, but it will become square as the amplifier reaches its output limits. The ring oscillator is a distributed version of the delay oscillator. The ring oscillator uses an odd number of inverters to give the effect of a single inverting amplifier with a gain of greater than one. Rather than having a single delay element, each inverter contributes to the delay of the signal around the ring of inverters, hence the name ring oscillator. Adding pairs of inverters to the ring increases the total delay and thereby decreases the oscillator frequency. Changing the supply voltage changes the delay through each inverter, with higher voltages typically decreasing the delay and increasing the oscillator frequency. Vratislav describes some methods of frequency-stability and power consumption improving of the CMOS ring-oscillator.

**Advantage:**

* Very compact & easy to integrate,compared to on-chip LC oscillators
* Very Wide tuning range
* Easy to get Multi-phase output
* Relatively power efﬁcient

**Application of VCO:**

* In Phase Locked Loops (PLLs), Frequency synthesis
* Clock and Data recovery circuits
* VCO based A/D converters
* Wired transceivers - Gigabit Ethernet, 10Gbit ethernet (IEEE802.3ae), SONET..
* Ultra Wide Band RF transceivers (3-5 GHz)
* Generation of clock/timing signals (CPU, DSP, DRAM..)

**Limitation of VCO:**

* Poor frequency stability
* Poor phase noise
* Performance more vulnerable to PVT variations
* Extremely high frequencies are difﬁcult to achieve

**Application of PLL:**

* PLLs are used in telecommunications, computers, radio and other electronic applications.
* They are frequently used in wireless communication, primarily on frequency modulation (FM) or phase modulation (PM) transmissions.
* Phase-locked loops are more commonly used for digital data transmission than for analog transmission and are more commonly manufactured as integrated circuits, although discrete circuits are used for microwave signal processing.